1-11 (Cancelled).

12. (Currently Amended) A method of forming a memory device, said method comprising:

patterning a trench ~~is~~ in a substrate;

filling a lower portion of said trench with a capacitor conductor;

forming a first conductive buried strap in said substrate adjacent a top portion of said capacitor conductor;

forming a doped trench top oxide in said trench above said capacitor conductor; and

after forming said first conductive buried strap and forming said doped trench top oxide, heating said ~~structure~~ device to form a second conductive buried strap in said substrate adjacent and connected to said first conductive buried strap ~~trench top oxide~~.

13. (Original) The method in claim 12, wherein said process of depositing said doped trench top oxide comprises a high density plasma-chemical vapor deposition (HDP-CVD) process.

14. (Currently Amended) The method in claim 12, wherein said process of depositing said doped trench top oxide comprises the following parameters:

deposition rate of silane reactant gas flow 10 - 75 sccm;

approximate bias plasma power between 300 ~~B~~ and 1000 W; and

phosphine gas delivery at gas flows below 5 sccm.

15. (Original) The method in claim 12, wherein during said process of depositing said doped trench top oxide layer, a percentage by weight of dopant in said doped trench top oxide layer is less than 1%.

16. (Original) The method in claim 12, further comprising depositing an undoped trench top oxide in said trench above said doped trench top oxide.

17. (Original) The method in claim 16, further comprising depositing a gate conductor in said trench above said undoped trench top oxide layer, wherein said undoped trench top oxide layer insulates said gate conductor from said capacitor conductor.

18. (Currently Amended) A method of forming a memory device, said method comprising:

patterning a trench ~~is~~ in a substrate;

filling a lower portion of said trench with a capacitor conductor; ~~and~~

forming a conductive buried strap in said substrate adjacent a top portion of said capacitor conductor;

forming a trench top oxide in said trench above said capacitor conductor, wherein said forming of said trench top oxide includes ~~depositing~~ forming a doped trench top oxide layer above said capacitor conductor, and forming an undoped trench top oxide layer above said doped trench top oxide layer; and

after forming said first conductive buried strap and forming said doped trench top oxide

layer, heating said device to form a second conductive buried strap in said substrate adjacent and connected to said first conductive buried strap.

19. (Original) The method in claim 18, further comprising depositing a conductive node strap in said trench adjacent said capacitor conductor.

20. (Canceled).

21. (Original) The method in claim 18, wherein said process of depositing said doped trench top oxide layer comprises a high density plasma-chemical vapor deposition process.

22. (Original) The method in claim 18, wherein during said process of depositing said doped trench top oxide layer a percentage by weight of dopant in said doped trench top oxide layer is less than 1%.

23. (New) The method in claim 12, wherein said forming of said first conductive buried strap comprises a first heating process that occurs when said doped trench top oxide is formed.

24. (New) The method in claim 18, wherein said forming of said conductive buried strap comprises a first heating process that occurs when said doped trench top oxide layer is formed.

25. (New) A method of forming a memory device, said method comprising:

patterning a trench is a substrate;

filling a lower portion of said trench with a capacitor conductor;

forming a doped material comprising first doping impurities adjacent a top of said capacitor conductor;

performing a first heating process to form a first conductive buried strap in said substrate adjacent a top portion of said capacitor conductor;

forming a doped trench top oxide comprising second doping impurities in said trench above said capacitor conductor; and

after forming said first conductive buried strap, performing a second heating process to form a second conductive buried strap in said substrate adjacent and connected to said first conductive buried strap.

26. (New) The method in claim 25, wherein said process of forming said doped trench top oxide forms said doped trench top oxide to a level above a top of said first conductive buried strap.

27. (New) The method in claim 25, wherein said first conductive buried strap and said second conductive buried strap combine to form a conductive path.

28. (New) The method in claim 25, wherein said first conductive buried strap is formed from

said first doping impurities outdiffusing into said substrate from said doped material, and said second conductive buried strap is formed from said second doping impurities outdiffusing into said substrate from said doped trench top oxide.

29. (New) The method in claim 25, wherein said first heating process occurs when said doped trench top oxide is formed.

30. (New) The method in claim 25, further comprising depositing an undoped trench top oxide in said trench above said doped trench top oxide.

31. (New) The method in claim 29, further comprising depositing a gate conductor in said trench above said undoped trench top oxide layer, wherein said undoped trench top oxide layer insulates said gate conductor from said capacitor conductor.